WHAT IS CLAIMED IS:

1. A device for inhibiting fluctuation of power supply voltage that is supplied to a plurality of internal circuits, wherein the internal circuits are operated in accordance with a plurality of clock signals, the device comprising:

a power fluctuation measuring circuit for measuring fluctuation peaks in the power supply produced when the internal circuits are operated and generating a measuring signal; and

a clock signal control circuit connected to the power fluctuation measuring circuit to adjust phases of the clock signals provided to respective ones of the internal circuits so that the fluctuation peaks in the power supply voltage produced when the internal circuits are operated are substantially offset by one another.

2. The device according to claim 1, wherein the clock signal control circuit includes:

a plurality of delay circuits, each connected to a respective one of the internal circuits, wherein each of the delay circuits selects the phase of the respective clock signal in accordance with a corresponding selection signal and provides the clock signal having the selected phase to the associated internal circuit; and

a control circuit connected to the power fluctuation measuring circuit to generate the selection signal in accordance with the measuring signal and provide the selection signal to the respective delay circuit so that the peaks are minimized.

3. The device according to claim 2, wherein the

control circuit sequentially switches the selection signals provided to the respective delay circuits to determine the selection signal that minimizes the peaks in accordance with the measuring signal generated by measuring the peaks whenever the selection signals are switched.

4. The device according to claim 2, wherein the control circuit provides the power fluctuation measuring circuit with a digital signal, the power fluctuation measuring circuit including:

a D/A converter connected to the control circuit for converting the digital signal to an analog reference voltage;

a peak hold circuit for holding the peaks of the power supply voltage; and

a comparator connected to the D/A converter and the peak hold circuit for comparing the analog reference voltages with the held peaks to generate the measuring signal.

5. The device according to claim 4, wherein the D/A converter generates an analog high reference voltage and an analog low reference voltage based on the digital signal, the peak hold circuit holds a high potential peak and a low potential peak of the power supply voltage, and the comparator compares the analog high reference voltage with the held high potential peak to generate a first measuring signal and compares the analog low reference voltage with the held low potential peak to generate a second measuring signal.

6. The device according to claim 1, wherein the plurality of internal circuits include a first internal

circuit and a second internal circuit, the device further comprising:

a delay circuit connected between the first and second internal circuits to provide a signal of the first internal circuit to the second internal circuit at a delayed time that is substantially the same as the difference between the phase of the clock signal provided to the first internal circuit and the phase of the clock signal provided to the second internal circuit.

7. A semiconductor device comprising:

a plurality of internal circuits, each operated in accordance with a respective one of a plurality of clock signals;

an inhibiting device for inhibiting fluctuation of power supply voltage that is supplied to the internal circuits, wherein the inhibiting device includes:

a power fluctuation measuring circuit for measuring fluctuation peaks in the power supply produced when the internal circuits are operated and generating a measuring signal; and

a clock signal control circuit connected to the power fluctuation measuring circuit to adjust phases of the clock signals provided to respective ones of the internal circuits so that the fluctuation peaks in the power supply voltage produced when the internal circuits are operated are substantially offset by one another.

8. The semiconductor device according to claim 7, wherein the inhibiting device and the internal circuits are configured on the same substrate.

9. The device according to claim 7, wherein the clock signal control circuit includes:

a plurality of delay circuits, each connected to a respective one of the internal circuits, wherein each of the delay circuits selects the phase of the respective clock signal in accordance with a corresponding selection signal and provides the clock signal having the selected phase to the associated internal circuit; and

a control circuit connected to the power fluctuation measuring circuit to generate the selection signal in accordance with the measuring signal and provide the selection signal to the respective delay circuit so that the peaks are minimized.

10. The device according to claim 9, wherein the control circuit sequentially switches the selection signals provided to the respective delay circuits to determine the selection signal that minimizes the peaks in accordance with the measuring signal generated by measuring the peaks whenever the selection signals are switched.

11. The device according to claim 9, wherein the control circuit provides the power fluctuation measuring circuit with a digital signal, the power fluctuation measuring circuit including:

a D/A converter connected to the control circuit for converting the digital signal to an analog reference voltage;

a peak hold circuit for holding the peaks of the power supply voltage; and

a comparator connected to the D/A converter and the peak hold circuit for comparing the analog reference voltages with the held peaks to generate the measuring

signal.

12. The device according to claim 11, wherein the D/A converter generates an analog high reference voltage and an analog low reference voltage based on the digital signal, the peak hold circuit holds a high potential peak and a low potential peak of the power supply voltage, and the comparator compares the analog high reference voltage with the held high potential peak to generate a first measuring signal and compares the analog low reference voltage with the held low potential peak to generate a second measuring signal.

13. The device according to claim 7, wherein the plurality of internal circuits include a first internal circuit and a second internal circuit, the device further comprising:

a delay circuit connected between the first and second internal circuits to provide a signal of the first internal circuit to the second internal circuit at a delayed time that is substantially the same as the difference between the phase of the clock signal provided to the first internal circuit and the phase of the clock signal provided to the second internal circuit.

14. A method for inhibiting fluctuation of power supply voltage that is supplied to a plurality of internal circuits, the method comprising:

providing a plurality of internal circuits with a plurality of clock signals, respectively; and

adjusting phases of the clock signals to substantially offset a plurality of fluctuation peaks of the power supply voltage that are produced when the internal circuits are

operated.

15. A method for inhibiting fluctuation of power supply voltage that is supplied to a plurality of internal circuits including a relatively large first internal circuit and relatively small second internal circuits, the method comprising:

providing the plurality of internal circuits with a plurality of clock signals, respectively; and

adjusting phases of the clock signals to substantially offset a first peak in the fluctuation of the power supply voltage that is produced when the first internal circuit is operated with second peaks in the fluctuation of the power supply voltage that are produced when the second internal circuits are operated.

16. A method for inhibiting fluctuation of power supply voltage that is supplied to an n number of digital circuits, the method comprising:

providing an n number of clock signals to the n number of digital circuits, respectively; and

when a cycle of noise produced in the power supply voltage during operation of each digital circuit is 2/n of a cycle of the respective clock signal, offsetting a plurality of fluctuations of the power supply voltage produced with the n number of digital circuits by deviating cycles of the n number of clock signals from one another by 1/n of a cycle.